WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising a functional block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the functional block,

the negative voltage generation circuit having

a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and

a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part,

wherein ground voltage is used as the reference voltage.

2. The semiconductor integrated circuit according to claim 1, wherein the charge pump part comprises

a self-oscillating circuit, which generates a predetermined pulse signal only during a period in which an output signal from the voltage detection part is in an activated state, and

a timing signal generation circuit, which converts the output pulse signal from the self-oscillating circuit into a timing signal,

and wherein the voltage detection part comprises

a constant voltage generation circuit,

a measuring voltage generation circuit, which receives an output voltage from the constant voltage generation circuit and an output voltage from the charge pump part and generates a divided measuring voltage by resistive means,

a first comparator for outputting the result of comparison after comparing the measuring voltage from the measuring voltage generation circuit with the ground voltage, and

an output buffer circuit for amplifying the compared result from the first comparator and outputting it to the charge pump part.

3. The semiconductor integrated circuit according to claim 1, wherein the voltage detection part comprises transistors and among the transistors included in the voltage detection part, all the voltage applied to substrates of N-channel transistors are set as ground voltage.

4. The semiconductor integrated circuit according to claim 2, wherein the voltage detection part has a voltage supplying circuit including a second comparator and a P-channel transistor interposed between the constant voltage generation circuit and the measuring voltage generation circuit,

wherein the voltage supplying circuit outputs a voltage based on the output voltage of the constant voltage generation circuit according to a configuration in which an output from the constant voltage generation circuit is supplied to an inverting input terminal of the second comparator, a power source voltage is supplied to a drain terminal of the P-channel transistor, an output from the second comparator is supplied to a gate terminal of the P-channel transistor, a source terminal of the P-channel transistor is coupled to a non-inverting input terminal of the second comparator, and an output from the source terminal of the P-channel transistor is coupled to the measuring voltage generation circuit.

5. The semiconductor integrated circuit according to claim 4, wherein the functional block comprises a memory block.

6. The semiconductor integrated circuit according to claim 2, wherein the first comparator has a first differential amplifier, a second differential amplifier and a third differential amplifier,

wherein the measuring voltage is supplied to one input terminal of the first differential amplifier while ground voltage is supplied to the other input terminal,

ground voltage is supplied to one input terminal of the second differential amplifier while the measuring voltage is supplied to the other input terminal,

an output voltage of the first differential amplifier is supplied to one input terminal of the third differential amplifier while an output voltage of the second differential amplifier is supplied to the other input terminal, and the output voltages from the first and the second differential amplifiers have reversed phases.

7. The semiconductor integrated circuit according to claim 2, wherein the constant voltage generation circuit has first voltage regulation means for regulating an output voltage by changing an output current value through a

change in the size of transistors included in a current mirror circuit, and the measuring voltage generation circuit has second voltage regulation means for changing a measuring voltage by changing the resistance of the resistive means.

8. The semiconductor integrated circuit according to claim 7, wherein the resistive means include a first resistor to a nth resistor serially-connected to each other, and the second voltage regulation means includes a first fuse to a nth fuse parallel-connected to each of the first resistor to the nth resistor,

wherein, when the resistance of the first resistor parallel-connected to the first fuse is defined as R, the resistance of the nth resistor parallel-connected to the nth fuse is set as $2^{(n-1)}$ times R, and the second voltage regulation means changes the measuring voltage by disconnecting at least one of the first to nth fuses and changing increments of the resistance from R to $2^{(n-1)}$ times R.

9. The semiconductor integrated circuit according to claim 2, wherein the first comparator of the voltage detection part includes transistors having a thicker gate oxide film than that of transistors used for a circuit in a stage preceding the first comparator in the voltage detection part.

10. The semiconductor integrated circuit according to claim 2, wherein the output buffer circuit of the voltage detection part has inverters in a plurality of stages where an inverter in a first stage includes transistors having a thicker gate oxide film than that of each inverter in other stages.

11. The semiconductor integrated circuit according to claim 1, wherein the functional block comprises a plurality of functional blocks respectively having different functions, and the negative voltage generation circuit comprises a plurality of negative voltage generation circuits for generating different predetermined negative voltages to be supplied to each of the plurality of functional blocks and a constant voltage generation circuit common to each of the plurality of negative voltage generation circuit.

13. A method for inspecting a semiconductor integrated circuit, the semiconductor integrated circuit comprising a functional block and a negative voltage generation circuit for generating a predetermined negative voltage to

be supplied to the functional block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage, the test method comprising

performing a test by externally applying a predetermined voltage to the functional block,

judging whether the functional block is defective based on the results of the test, and

supplying a predetermined negative voltage from the negative voltage generation circuit only for the functional block judged as non-defective.

14. A method for inspecting a semiconductor integrated circuit, the semiconductor integrated circuit comprising a functional block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the functional block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage, the test method comprising

performing a test by externally applying a predetermined voltage to be output by the negative voltage generation circuit to the functional block,

judging whether the functional block is defective based on the results of the test and recording voltage conditions optimizing operating conditions of the functional block,

connecting the negative voltage generation circuit whose output voltage is regulated to the voltage conditions only to the functional block judged as non-defective, and performing test items of the functional block by supplying a negative voltage.

15. A recording device comprising a semiconductor integrated circuit, the semiconductor integrated circuit comprising a functional block and a negative voltage generation circuit for generating a predetermined negative voltage to

be supplied to the functional block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage,

wherein the recording device comprises a recording system using at least one selected from light and magnetism.

16. Communication equipment comprising a semiconductor integrated circuit, the semiconductor integrated circuit comprising a functional block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the functional block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage.

17. A method for inspecting a semiconductor integrated circuit, the semiconductor integrated circuit comprising a memory block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the memory block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage, the test method comprising

performing a test by externally applying a predetermined voltage to the memory block,

judging whether the memory block is defective based on the results of the test, and

supplying a predetermined negative voltage from the negative voltage generation circuit only for the memory block judged as non-defective.

18. A method for inspecting a semiconductor integrated circuit, the semiconductor integrated circuit comprising a memory block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the memory block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage, the test method comprising

performing a test by externally applying a predetermined voltage to be output by the negative voltage generation circuit to the memory block,

judging whether the memory block is defective based on the results of the test and recording voltage conditions optimizing operating conditions of the memory block,

connecting the negative voltage generation circuit whose output voltage is regulated to the voltage conditions only to the memory block judged as non-defective, and performing test items of the memory block by supplying a negative voltage.

19. A recording device comprising a semiconductor integrated circuit, the semiconductor integrated circuit comprising a memory block and a negative voltage generation circuit for generating a predetermined negative voltage to be supplied to the memory block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage,

wherein the recording device comprises a recording system using at least one selected from light and magnetism.

20. Communication equipment comprising a semiconductor integrated circuit, the semiconductor integrated circuit comprising a memory block and a negative voltage generation circuit for generating a predetermined negative

voltage to be supplied to the memory block, the negative voltage generation circuit having a charge pump part, which converts a power source voltage into the predetermined negative voltage and outputs it, and a voltage detection part, which controls the output voltage of the charge pump part by comparing the output voltage of the charge pump part with a reference voltage and outputting the result of comparison to the charge pump part, wherein ground voltage is used as the reference voltage.